Logic Gates and Digital Signals

Introduction: A fundamental component of digital electronic devices is the logic gate. This Tech Note discusses some basic operational details about logic gates and how digital signals are processed. Digital devices are not concerned about the level of an input signal, they are only concerned as to whether there is an input signal or not. They operate on the basis of yes or no. Electronic switching devices can be installed in an electrical circuit to make decisions and bring about actions based upon the device's observation of the status of a circuit. These devices are super smart and can count from "zero" all the way up to "one". A common circuit operating voltage is nominal +5 volts dc. When a wire is energized at + 5 Vdc it is considered to be at the "one" (1) state. When a wire is connected to ground (0 volts dc) it is considered to be at the "zero" (0) state. A wire or terminal not connected to zero or +5 Vdc may cause unpredictable results.

   Since the only two states for wires and terminals within the circuit are "one" (+5 Vdc) and "zero" (ground), then these devices operate in "binary". They can do math and make decisions using "binary numbering" provided binary algorithms can be worked out to perform the task. Math based upon binary numbering is called Boolean math. It is important to know the basic logic gate functions, and to be able to write a Boolean expression for those functions. For details on logic gates and Boolean math refer to Tech Note 542 and for details on numbering systems used with electronic devices refer to Tech Note 536.

Understanding Boolean variables: A group of wires sometimes called a *bus* carry digital information from one location to another. Each wire of the bus either carries a voltage (one state) or is grounded (zero state). Each wire or line is often called a *bit*. The number of wires in a bundle or bus (number of bits) are usually in multiples of four, such as four, or eight, or twelve, or sixteen.   Assume a decision is to be made based upon the status of a binary 4-bit bus (nibble). Decimal numbers can be represented in binary form by assuming a value for each wire of the binary bus. The values of each wire starting with the first is the number two raised to a power. The first wire is 2^0 which is the value 1. The second is 2^1 which is 2. The third is 2^2 which is 4, and the fourth is 2^3 which is 8.   Starting with the "one line" identify each wire with a letter.

   2^0 or 1 line is at the 1 state ----------- A
   2^1 or 2 line is at the 1 state ----------- B
   2^2 or 4 line is at the 1 state ----------- C
   2^3 or 8 line is at the 1 state ----------- D

   When there is a voltage on a "line" we will identify it's status by the letter, such as "A", and it is considered to be at the "one" state. If the line is at the "zero" state we will refer to that same line as "NOT A". This condition is represented by the letter with a horizontal line above it, such as $\overline{A}$.

   Example: Assume the above 4-bit bus is displaying the digital number 10 in binary. From D to A the bus will be 1010. D is at the 1 state, C is at the zero state, B is at the one state and A is at the zero state. Assign each bit in the digital bus the following values and

multiply it by the decimal value of that bit to verify that the binary number is properly representing the digital number. The values are $\overline{A} = 0$, B = 1, $\overline{C} = 0$, and D = 1. Multiply the value of the bit by the status of the bit and add the numbers to obtain the decimal equivalent. (0 x 1) + (1 x 2) + (0 x 4) + (1 x 8) = 10.

$\overline{A}$, B, $\overline{C}$, D = 10   (left of the equals is binary, right of the equals is decimal)

The Inverter: In binary math "zero" and "one" are considered "complements" of each other. A and $\overline{A}$ are complements of each other. Sometimes when a logic device is installed a decision is based upon the state of an input, but in order for the gate or device to function it must be supplied with the complement. Switching the status of a line to it's complement is called "inversion." The electronic device that does this is called an *inverter*. It has one input and one output. The symbol for an "inverter" is shown in Figure 541.1. An inverter is a small triangle with a small circle at the point. When a circle is drawn at the input of some electronic chips, the circle means the input is inverted as it enters the chip circuitry.
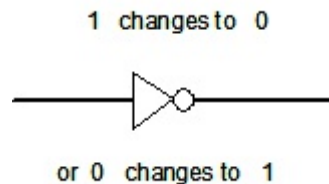
1 changes to 0

or 0 changes to 1

Figure 541.1 An inverter has one input and one output. The output of the inverter is the complement of the input. A zero is changed to a one, and a one is changed to a zero.

Basic Logic Operations: A logic gate is an electronic device with two or more inputs and one output. There are two logic states for the wires in a digital circuit, either zero or one. If the wire or terminal is grounded it is at the zero state. If the wire or terminal has a positive voltage present above some threshold level it is considered to be at the one state. Logic gates are commonly available with two, three, and four inputs and one output. There are two basic logic operations, OR, and AND. For simplicity only 2-input gates will be considered at this point. A two input OR gate is shown in Figure 541.2.
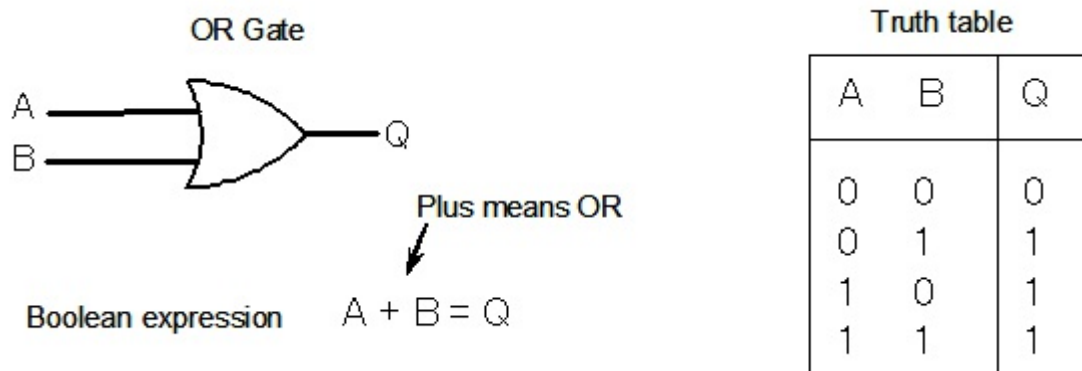
OR Gate

Plus means OR

Boolean expression $A + B = Q$

Truth table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

Figure 541.2 A two input OR gate is shown along with it's truth table and Boolean expression.

First consider the two input OR gate. If both inputs are zero, the output of the gate will be zero. If any one or both of the inputs are at the one state, the output will be at the one state. The symbol for a two input OR gate is shown in Figure 541.2. Remember the shape of the gate symbol. Inputs are on the left labeled A and B, and the output is on the right labeled Q. A truth table is also provided which gives all of the possible combinations of the inputs and the output that results form each combination. A Boolean math expression is shown for the two input OR gate with the plus sign designating the OR operation. Each row in the truth table represents one combination of the Boolean math expression. Read the expression as follows: A or B equals Q, zero or zero equals zero, zero or one equals one, one or zero equals one, one or one equals one.

In the case of an AND gate both inputs must be at the one state at the same time in order for the output to be at the one state. Figure 541.3 shows the symbol for a two input AND gate along with the truth table and Boolean expression. A times symbol or a dot signifies an AND operation. In a more complex Boolean expression portions of an equation may be surrounded with parentheses such as $(A + B)(C + D)$. Each individual operation within the parentheses is an OR operation, but the two individual parentheses operations are an AND. The dot between them is assumed. The Boolean expression in Figure 541.3 is read A and B equals Q. The output Q is at the one state only when both A and B are at the one state. Otherwise the output is zero.
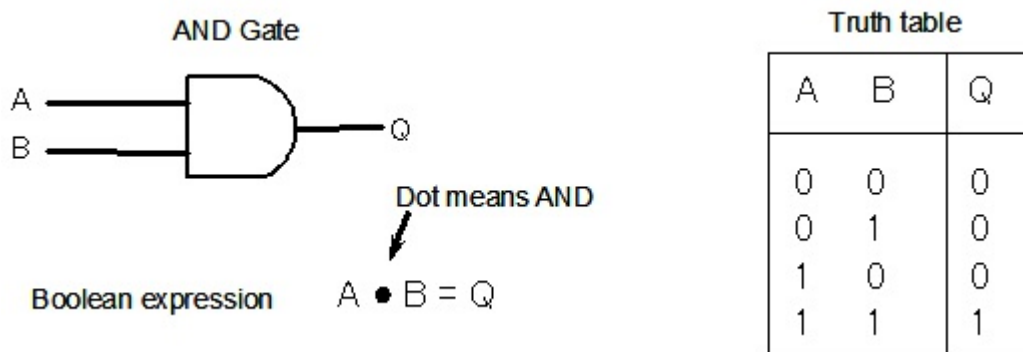
AND Gate

Truth table

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

Dot means AND

Boolean expression $A \bullet B = Q$

Figure 541.3 *A two input AND gate is shown along with it's truth table and Boolean expression.*

NOT OR and NOT AND gates: Adding an inverter to the output of an OR gate or an AND gate creates two additional very useful gates. The output of the gate is inverted or opposite to that of the two basic gates previously discussed. With the Boolean expression, rather than the output shown as Q it is shown with a line above, $\overline{Q}$, or in the case or a NOT OR operation the expression may be shown as follows: $\overline{A+B}$. Rather than calling the operation a NOT OR the expression is shortened to NOR. The inverter is within the chip, however, an inverter could be added to the output of an OR chip to accomplish the same result. A two input NOR gate is shown in Figure 541.4 along with the truth table and the Boolean expression. Compare the truth table of Figure 541.4 with the truth table of Figure 541.2 and note the outputs Q are opposite.

The NOT AND gate is simply an AND gate with an inverter at the output. The output is just the opposite as with the AND gate. Rather than calling the operation a NOT AND the term is shortened to NAND. A two input NAND gate symbol along with the truth table and Boolean expression are shown in Figure 541.5.
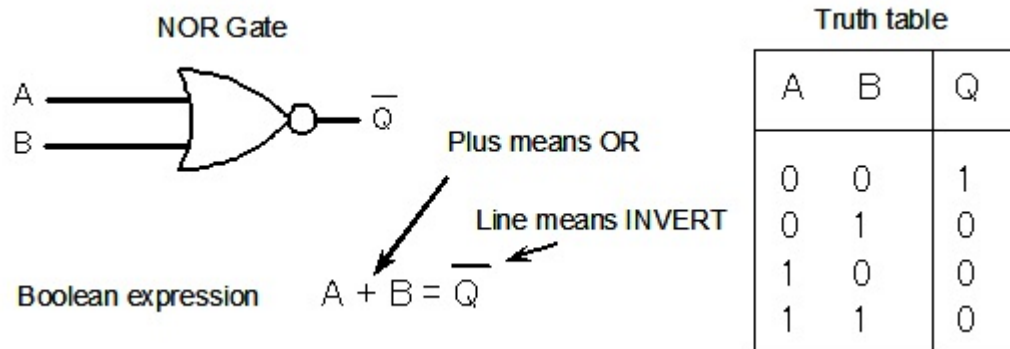
NOR Gate

Truth table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

Plus means OR

Line means INVERT

Boolean expression $A + B = \overline{Q}$

Figure 541.4 *A two input NOR gate is shown along with it's truth table and Boolean expression.*

AND Gate

Truth table

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

Dot means AND

Line means INVERT

Boolean expression $A \bullet B = \overline{Q}$
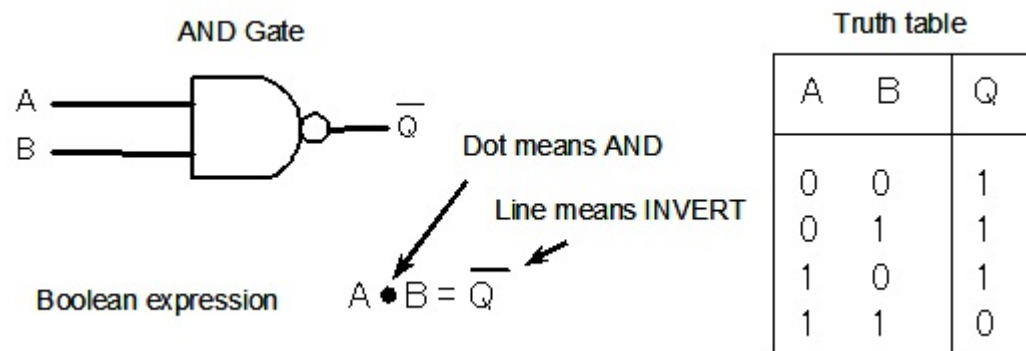
Figure 541.5 *A two input NAND gate is shown along with it's truth table and Boolean expression.*

Exclusive OR gate: A two input OR gate will give an output of one if either or both of the inputs are at the one state. Sometimes an output of one is only desired when either input is at the one state but not both. A gate is made that can accomplish this operation and it is called the exclusive OR gate. The symbol for an exclusive OR gate is shown in Figure 541.6 along with the truth table and the Boolean expression. The circle with the plus sign inside signifies an exclusive OR operation.

Gates on a Chip: Gates are a key component of digital electronic devices, but frequently they are needed as individual components to be installed within a circuit to perform a needed function or to make a decision based upon the requirements of a circuit. Electronic devices are available in a number of different formats, but for now the gates that will be considered is what is known as the 7400 series TTL format. The gates are readily available as a 14 pin DIP or dual in-line parallel configuration which means 14 terminals or pins, seven on a side. The inverter and five common 2-input gate chips are shown in Figure 541.7. The chip numbers are standardized within the industry. The gate diagram is not on the chip. Diagrams can easily be found on the web. There will be a dot or a notch on one end of the chip. Arrange the chip so the dot or notch is at the top and the pin numbers will start at the upper left and increase in a counter-clockwise direction. Each of these chips must be provided with a source of power in

order to operate. Standard voltage for these chips, V_{CC}, is a nominal +5 Vdc which is connected to pin 14 on all of these chips. Pin 7 must be connected to common or ground.
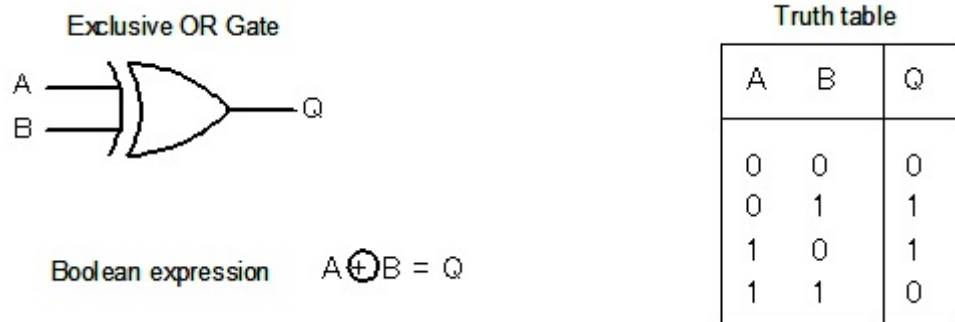

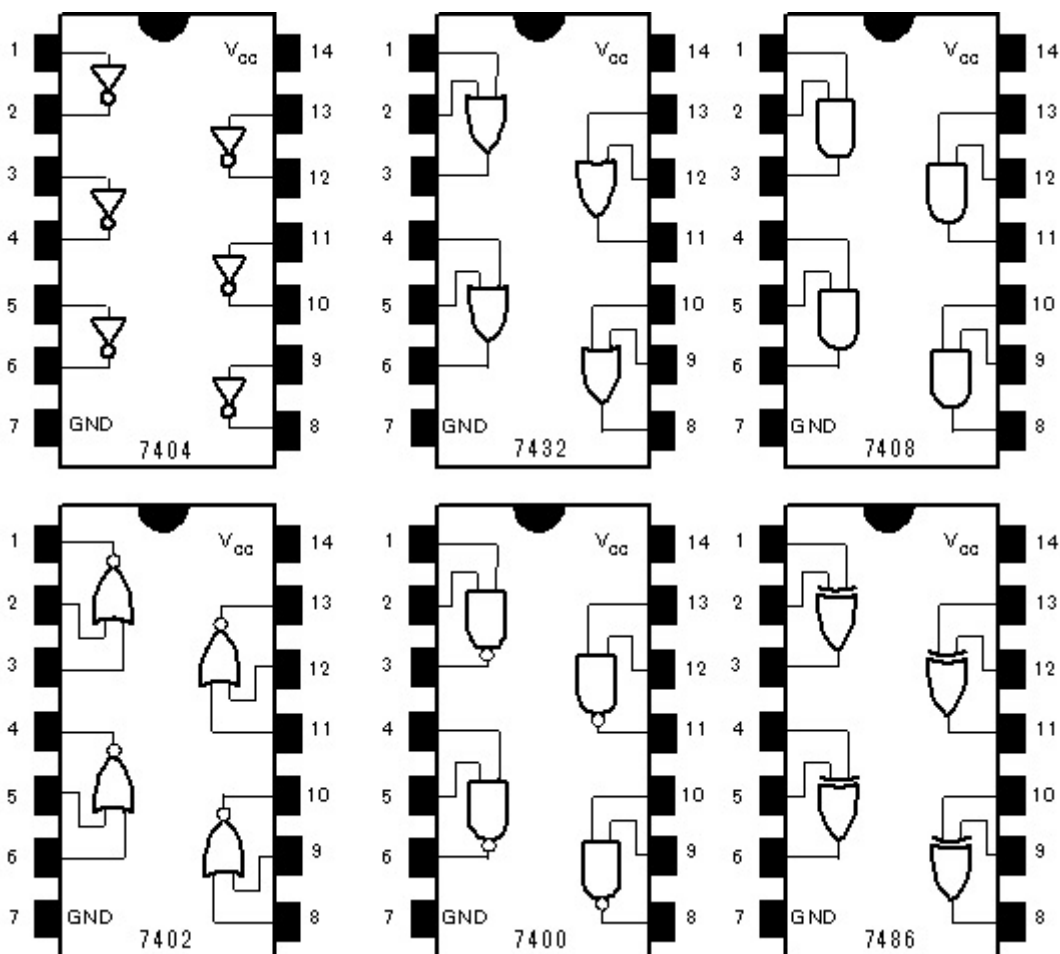**Figure 541.6** *An Exclusive OR gate is shown along with it's truth table and Boolean expression.*

Figure 541.7 *Inverter and logic gates available on 14 pin DIP chips in TTL format.*

Gates with too many inputs: What if the gate available for a project has more inputs than needed? The problem can be easily solved as illustrated in Figure 541.8. The unused input or inputs are either tied to the zero state or the one state depending upon the type of logic gate. The gates in Figure 541.8 are 3-input gates, but only two inputs are needed. In the case of an OR or NOR gate the unused input is tied to the zero state (ground). In the case of the AND and NAND gate, one input is tied to the one state (+5 Vdc).
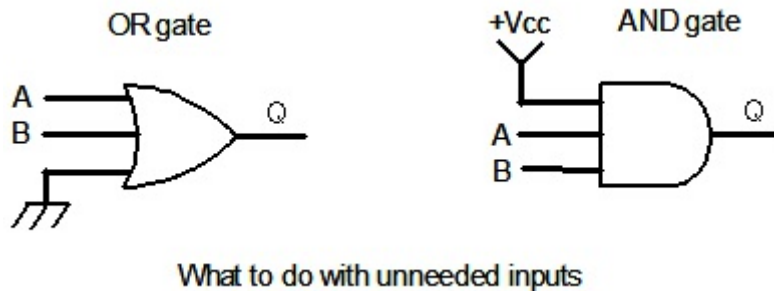

Figure 541.8 *In the case of an OR or NOR gate any unneeded inputs are tied to ground, and in the case of an AND or NAND gate, any unneeded inputs are tied to +5 Vdc.*

Make an Inverter from a NOT gate: If an inverter is needed, but one is not available, an inverter can be made from a NAND or NOR gate. The inverter can be obtained in either of two ways. All of the inputs of the NOR or NAND gate can be tied together and used as a single input as shown in Figure 541.9. The output will be the complement of the input. Another way to obtain an inverter from a NOR gate is to tie all but one of the inputs to the zero state (ground). The output will be the complement of the input. In the case of an NAND gate, tie all but one of the inputs to the one state (+5 Vdc). The output will be the complement of the input.
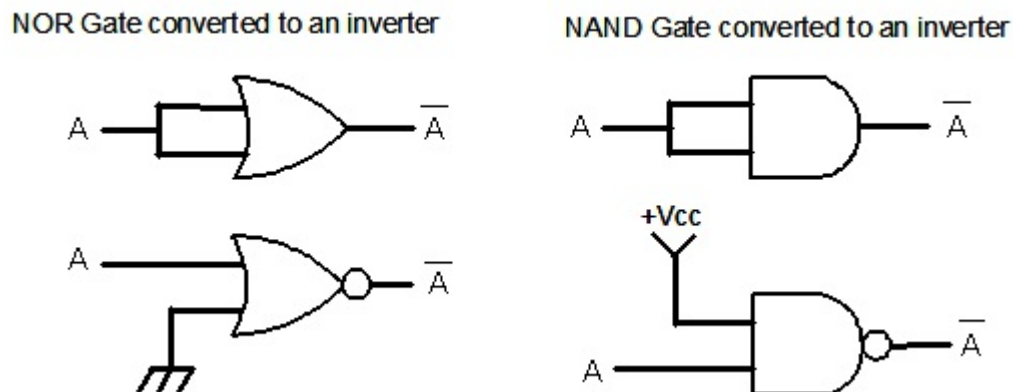

Figure 541.9 *A NOR or a NAND gate can be converted to an inverter by tying all of the inputs together to act as one input. A NOR gate is converted to an inverter by tying all but one on the inputs to ground. A NAND gate is converted to an inverter by tying all but one input to +5 Vdc.*

Not enough inputs: If more inputs are needed than are available on the logic gates available, then multiple gates can be connected in parallel to gain the desired number of inputs needed. This technique is illustrated in Figure 541.10. In the example of Figure 541.10, the circuit

requires four inputs, but the gates have only two inputs. The Boolean expression for making a four input OR gate from 2-input OR gates is shown. It is important to visualize the gates needed to satisfy a Boolean expression, and to write a Boolean expression from the gates in a circuit.
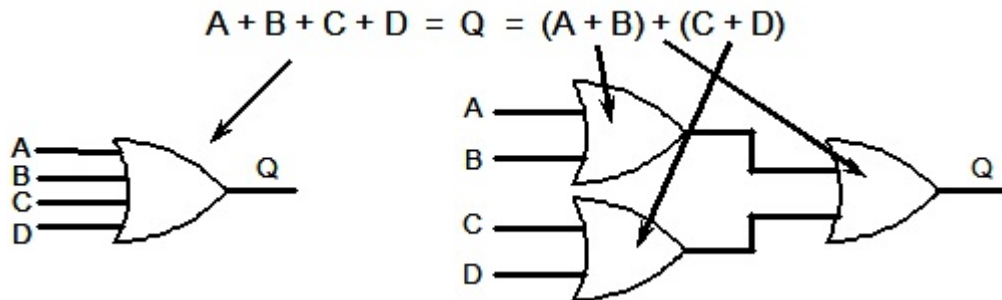
$$A + B + C + D = Q = (A + B) + (C + D)$$

Figure 541.10 *A 4-input OR gate is shown on the left and an equivalent constructed with 2-input OR gates on the right. The Boolean expression is shown with arrows pointing to the gate that is performing the Boolean operation.*

AND gates can be combined in the same manner as shown in the previous figure to construct an equivalent to a 4-input AND gate using 2-input AND gates. In Figure 541.11, however, two previous techniques are combined to illustrate the versatility of combining gates to create a desired circuit. For the example illustrated in Figure 541.11, a 3-input AND gate is needed, but only 2-input AND gates are available. Two AND gates are connected in parallel, but one input of one of the gates is not needed. That problem is solved by tying one input of one of the gates to +5 Vdc.
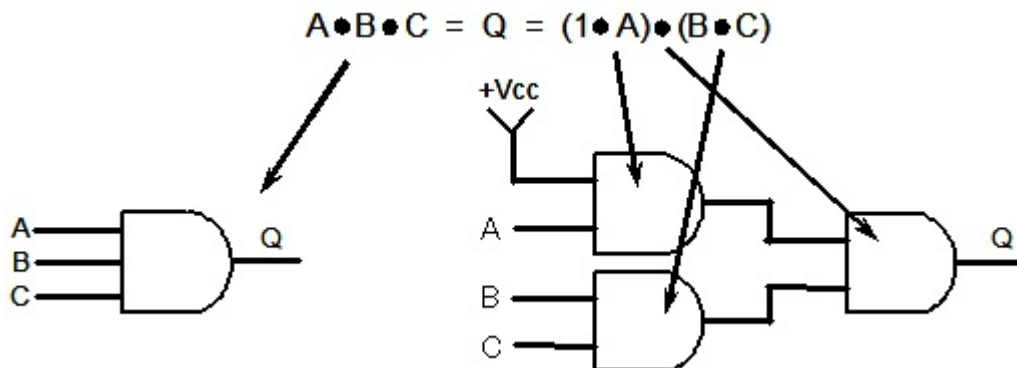
$$A \bullet B \bullet C = Q = (1 \bullet A) \bullet (B \bullet C)$$

Figure 541.11 *For this example a 3-input AND gate equivalent is constructed using 2-input AND gates, but one input of one of the gates must be tied to the one state.*

IC Chip Formats: Digital electronic devices are constructed mainly of logic gates. In order to compress the size of complex circuits to make them small enough to fit within something like a wrist watch or a portable hand-held calculator a technique needed to be developed for directly coupling the components on a single silicon chip. The result was the advent of integrated circuits or the IC. One method of a complete logic gate on a single chip was with the use of bi-polar junction transistors. When several bi-polar junction transistors are coupled together to perform a function there will be resistors in the circuit between the transistors, such as in the

case of a common emitter NPN transistor with a resistor limiting current in the base circuit and another in the collector circuit. Eventually techniques were developed where most of these resistors could be eliminated and one bi-polar junction transistor could be directly coupled to the next. This has become known as transistor-transistor logic or TTL. A complete logic circuit such as an inverter or a NAND gate is constructed on one chip. The common logic gates are usually available with several independent gates of the same type on one chip and assembled within a single device. Manufacturers have standardized on a numbering system, and a common package for these chips is in the dual in line form such as those shown in Figure 541.7. Logic gates constructed with bi-polar junction transistors have a four-digit number beginning with the number 74 for the commercial grade and 54 for the military grade. Typically they are available with two, three, four, and eight inputs. They are fast switching, rugged, and can be handled without special tools, but they do consume power because of the nature of operation of a bi-polar junction transistor. They are not practical for batter operation.

A technique for assembling a complete logic gate on a single chip was developed using the metal oxide semiconducting field effect transistor or MOSFET. Basically a voltage is applied to a terminal called a gate and it creates a conducting channel between two semiconductor regions called the source and drain. One type is called a P-channel MOSFET and the other is called an N-channel MOSFET. By coupling the two together in a manner similar to that shown in Figure 541.12, an inverter can be created.
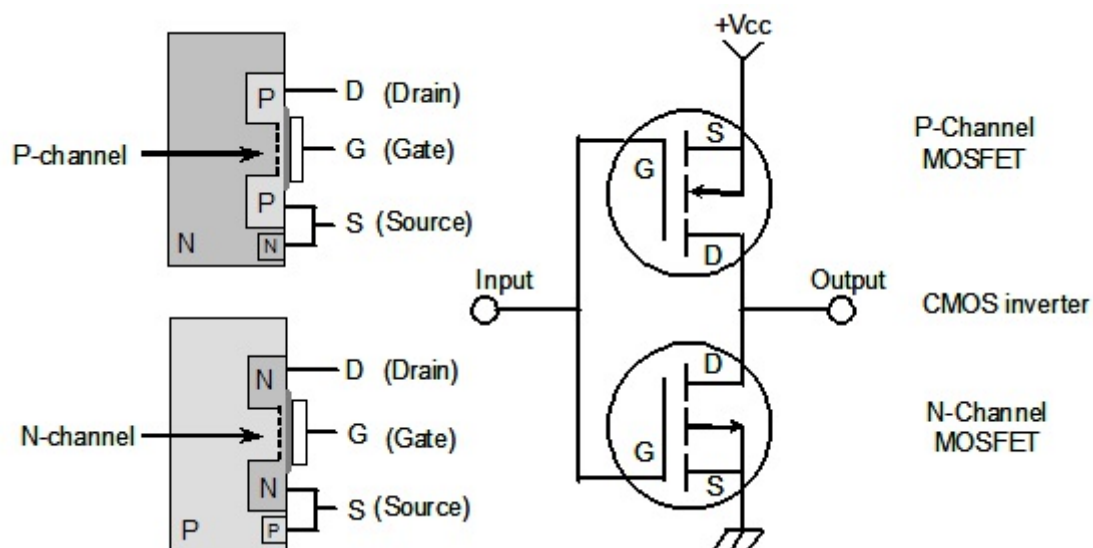

Figure 541.12 A simple logic inverter can be constructed using a P-channel and an N-channel MOSFET with the two drains connected together to form the output, the two gates connected together to form the input and the P-channel source connected to a plus voltage and the N-channel source connected to ground. Thus is formed a complementary metal oxide semiconductor inverter or CMOS inverter.

When one of the MOSFETs in Figure 541.12 is turned on the other will be turned off. When a plus voltage is applied to the input (both gates) the P-channel MOSFET turns off and the N-channel turns on connecting the output to ground or zero. With zero or ground applied to the input the P-channel MOSFET turns on, and the other turns off thus connecting the output to a plus voltage or one state. The P-channel MOSFET and the N-channel MOSFET are considered complements of each other, thus the name complementary metal oxide semiconductor chip or CMOS. Logic gates can be constructed on a single chip using the CMOS technique. A major advantage of the CMOS chip is that it operates with very little power

drain thus making it ideal for battery operation. A disadvantage is that the chips are voltage delicate meaning they are prone to damage due to static charge. When not installed they need to be stored in a material that electrically shorts the terminals together to prevent a voltage from developing between the terminals, and they should never be handled without special tools. The original CMOS chips had a slower switching speed than TTL chips, but those issues have been improved with time. Some CMOS chips are numbered in the 4000s. However, some have the numbers that begin with 74C, 74HC, and 74HCT.

Example Gate Application: This is an example of how a task is first written in a Boolean expression and then converted to an actual working circuit using gates. Consider the case of a four-wire digital bus where decimal numbers from zero to fifteen can be represented in binary form. Just for the sake of an example it is desired to flash a light every time the four bit but displays decimal 9 in binary. That is the bus status is D = 1, C = 0, B = 0, and A = 1. In order for the light to flash, the bus status must be D, and Not C, and Not B, and A. That is $D \cdot \overline{C} \cdot \overline{B} \cdot A = Q$. This is an AND operation since these conditions must be present at the same time.

   To further complicate the task, assume we only have 2-input and gates. That will involve two gates in parallel. One rule of Boolean math is that it does not matter what combination of inputs are at each gate. To study more about Boolean math, review Tech Note 542. The Boolean expression can be represented as 2-input gates: $D \cdot \overline{C} \cdot \overline{B} \cdot A = (D \cdot \overline{C}) \cdot (\overline{B} \cdot A)$.

   When decimal 9 is reached on the binary bus, an output (one state) at Q is needed and a zero state for all other binary combinations. In order for the AND gates to turn on and give an output there must be a one state at all inputs. How then can there be two one states at the inputs of the an AND gate when one input is zero? B and C are zero on the binary bus for the decimal number 9. The answer is an inverter at the input for B and C. When B and C are zero the inverter will place a 1 at the input to the gates. When B and C are at the one state, the inverter will put a zero at the inputs of the AND gates. The completed circuit is shown in Figure 541.13. There will be a one state output at Q only when the digital bus is at decimal 9 which in binary is 1 0 0 1.
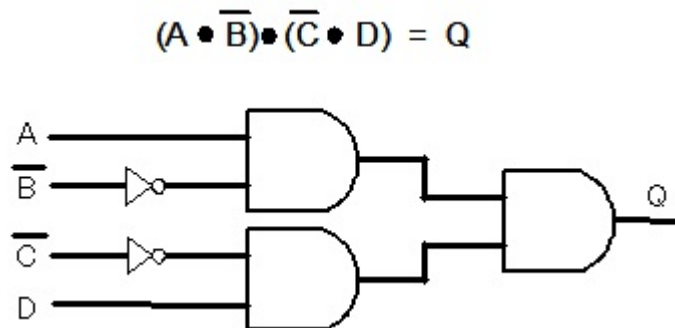
$$(A \cdot \overline{B}) \cdot (\overline{C} \cdot D) = Q$$

Figure 541.13 *These 2-input AND gates will only display a one state at the output when the binary bus is at decimal 9.*